FULL VERSION OF PENDING CLAIMS

1. (Currently Amended) A thin film transistor (TFT) array panel, comprising:

an insulating substrate;

first and second semiconductor members formed on the substrate and having opposite conductivity;

a first gate member formed on a first layer, insulated from the first and the second semiconductor members and overlapping one of the first and the second semiconductor members;

a second gate member formed on the [[same]] first layer ~~as the first gate member~~, separated from the first gate member, and insulated from the first and the second semiconductor members, the second gate member not overlapping the first and the second semiconductor members;

a first data member formed on a second layer, connected to one of the first and the second semiconductor members and insulated from the first and the second gate members; and

a first connection formed on the [[same]] second layer ~~as the first data member~~ and connecting the first gate member and the second gate member.

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2. (Original) The TFT array panel of claim 1, wherein the first and the second semiconductor members comprise polysilicon.

3. (Original) The TFT array panel of claim 2, wherein the first gate member overlaps the first semiconductor member.

4. (Currently Amended) The TFT array panel of claim 3, further comprising a third gate member formed on the first layer, separated from the first and the second gate members, insulated from the first and the second semiconductor members, and overlapping the second semiconductor member.

5. (Currently Amended) The TFT array panel of claim 4, further comprising a second connection formed on the [[same]] second layer ~~as the first data member~~ and connecting the second gate member and the third gate member.

6. (Currently Amended) The TFT array panel of claim 4, further comprising:

a fourth gate member formed on the first layer, separated from the first, the second, and the third gate members and insulated from the first and the second semiconductor members, the fourth gate member not overlapping the first and the second semiconductor members; and

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a second connection formed on the [[same]] second layer ~~as the first data member~~ and connecting the third gate member and the fourth gate member.

7. (Currently Amended) The TFT array panel of claim 6, further comprising:

fifth and sixth gate members formed on the first layer, separated from the first to the fourth gate members, insulated from the first and the second semiconductor members, and overlapping the first and the second semiconductor members, respectively;

a seventh gate member formed on the first layer, separated from the first to the sixth gate members and insulated from the first and the second semiconductor members, the seventh gate member not overlapping the first and the second semiconductor members; and

third and fourth connections formed on the [[same]] second layer ~~as the first data member~~ and connecting the fifth and the sixth gate members to the seventh gate member.

8. (Currently Amended) The TFT array panel of claim 7, further comprising a fifth connection formed on the [[same]] second layer ~~as the first data member~~ and connecting the first semiconductor member and the second semiconductor member.

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9. (Currently Amended) The TFT array panel of claim 8, further comprising:

third and fourth semiconductor members formed on the substrate and having opposite conductivity;

eighth and ninth gate members formed on the first layer, separated from the first to the seventh gate members, insulated from the first to the fourth semiconductor members, overlapping the third and the fourth semiconductor members, respectively; and

sixth and seventh connections formed on the [[same]] second layer ~~as the first data member~~ and connecting the fifth and the sixth gate members to the eighth and the ninth gate members, respectively.

10. (Currently Amended) The TFT array panel of claim 9, further comprising:

tenth and eleventh gate members formed on the first layer, insulated from the first to the fourth semiconductor members and overlapping the third and the fourth semiconductor members, respectively;

twelfth and thirteenth gate members formed on the [[same]] first layer ~~as the tenth and the eleventh gate members~~, separated from the first to the eleventh gate members, and insulated from the third and the fourth semiconductor members, the twelfth and the thirteenth gate members not overlapping the first to the fourth semiconductor members; and

eighth and ninth connections formed on the [[same]] second layer ~~as the first data member~~ and connecting the tenth and the

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eleventh gate members to the twelfth and the thirteenth gate members, respectively.

11. (Currently Amended) The TFT array panel of claim 10, further comprising a seventh connection formed on the [[same]] second layer ~~as the first data member~~ and connecting the third semiconductor member and the fourth semiconductor member.

12. (Original) The TFT array panel of claim 11, wherein the first data member is connected to the first and the third semiconductor members.

13. (Original) The TFT array panel of claim 12, further comprising a second data member connected to the second and the fourth semiconductor members and insulated from the first to the thirteenth gate members.

14. (Original) The TFT array panel of claim 13, wherein the first data member transmits a gate-off voltage for turning off a thin film transistor and the second data member transmits a gate-on voltage for turning on the thin film transistor.

15. (Original) The TFT array panel of claim 1, further comprising:

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a first insulating layer interposed between the first and the second semiconductor members and the first and the second gate members; and

a second insulating layer interposed between the first and the second gate members and the first data member,

wherein the second insulating layer has a first contact hole for connecting the first gate member and the second gate member, and the first and the second insulating layer has a second contact hole for connecting the first data member and the one of the first and the second semiconductor members.

16. (Currently Amended) A method of manufacturing a thin film transistor (TFT) array panel, the method comprising:

forming a blocking layer on a substrate;

depositing an amorphous silicon film on the blocking layer;

crystallizing the amorphous silicon film into a polysilicon film;

patterning the polysilicon film to form first and second polysilicon members;

forming a gate insulating layer on the first and the second polysilicon members;

forming a plurality of first conductive members overlapping the first and the second polysilicon members; [[and]]

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forming a plurality of second conductive members not overlapping the first and the second polysilicon members;

implanting N type impurity to form a plurality of N type impurity regions in the first polysilicon member;

implanting P type impurity to form a plurality of P type impurity regions in the second polysilicon member;

depositing an interlayer insulating layer on the first and the second conductive members and the N type and the P type impurity regions;

patterning the interlayer insulating layer and the gate insulating layer to form a plurality of first contact holes exposing portions of the first and the second conductive members and to form a plurality of second contact holes exposing portions of the N type and the P type impurity regions; [[and]]

forming a plurality of connections connected to the first and the second conductive members through the first contact holes; and

forming a plurality of data members connected to the N type and the P type impurity regions through the second contact holes.

17. (Original) The method of claim 16, wherein the N type impurity implantation precedes the P type impurity implantation.

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18. (Original) The method of claim 16, wherein the P type impurity implantation precedes the N type impurity implantation.

19. (Currently Amended) The method of claim 16, wherein the data members include first and second voltage ~~supplying~~ lines respectively connected to the N type and the P type impurity regions for transmitting first and second voltages.

20. (Original) The method of claim 19, wherein the data members include a connecting member connected to both the N type impurity region and the P type impurity region.

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